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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,776	KIM ET AL.	
	Examiner	Art Unit	
	Seokyun Moon	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of the Applicants' claim for foreign priority based on an application filed in South Korea on February 6, 2003. It is noted, however, that Applicants have not filed a certified copy of the foreign priority application, Appl. No. 2003-0007521, as required by 35 U.S.C. 119(b).

Claim Objections

2. **Claim 4** is objected to because of the following informalities: line 3, "*stored in the first and the color-specific second gamma voltage registers ...*".

For further examination purpose, it will be interpreted as "*stored in the first and the second color-specific gamma voltage registers ...*".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claims 12-21** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As to **claim 12**, the claim discloses "... *a gray voltage generator coupled to the pixel electrodes, ...*". However, as shown in fig. 4, the gray voltage generator is not coupled to the pixel electrodes but is coupled to the data driver, and the data driver is coupled to the pixel electrodes.

As best understood by Examiner, the claim limitation will be interpreted as "... *a gray voltage generator coupled to the data driver, ...*" for further examination purpose.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1, 2, 9, 10-13**, and **21-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (US 2002/0015028) in view of Kudo et al. (US 2006/0033695, herein after "Kudo").

As to **claim 1**, Park teaches an apparatus for driving a liquid crystal display [par. (0026) lines 1-3], the apparatus comprising:

a signal controller ("*controller 20*") [fig. 1] for generating digital signals for different pixel colors [par. (0034) lines 2-5];

a gray voltage generator (a combination of "*memory 32*", "*decoder 33*", and "*D/A converter 34*" included in a plurality of "*column driver IC 14*") [figs. 1 and 3] coupled to the signal controller, wherein the gray voltage generator generates gray voltage signals [par. (0038) lines 3-6]; and

a data driver (a combination of "*shift register 24*", "*data latch 26*", "*d/a converter 28*", and "*buffer 30*" included in a plurality of "*column driver IC 14*") [figs. 1 and 3] coupled to the gray voltage generator and the signal controller, wherein the data driver converts each one of the digital signals to a corresponding analog signal by selecting one of the gray voltage signals [par. (0037)].

Park does not teach the gray voltage generator generating gray voltage signals that are specific to the different pixel colors and the data driver converting each one of the digital signals to an analog signal by selecting one of the gray voltage signals that is associated with the same pixel color as the digital signal that is being converted.

However, Kudo teaches an apparatus for driving a liquid crystal display [par. (0002)] comprising a signal controller (a combination of "*MPU 906*", "*system interface 907*", and "*control register 301*") [fig. 16] generating digital signals, gray scale voltage generator ("*302*") coupled to the signal controller generating gray voltage signals that are specific to the different pixel colors [par. (0107) lines 1-4 and par. (0108) lines 6-10], and a data driver ("*decoder circuit 303*") selecting one of the gray voltage signals that is associated with the same pixel color as the digital signal.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the signal controller of Park to include a register storing gamma values for each of a plurality of pixel colors, to modify the gray voltage generator of Park to generate gray voltage signals that are specific to each of the plurality of pixel colors by including additional memory, decoder, and D/A converter for each of the plurality of pixel colors, and to modify the data driver of Park to select one of the gray voltage signals which is associated with the same pixel color as the digital signal outputted from the signal controller, as taught by Kudo, in order to supply gray

voltages representing more accurate gamma curves to the liquid crystal panel of the display of Park, and thus to improve the image quality of the display.

As to **claim 2**, Park as modified above teaches the gray voltage generator separately storing gray voltages for each of the pixel colors [Park: par. (0038) lines 1-2] (Note that the apparatus of park as modified above includes "*memory 32*" for each of the pixel colors).

Park as modified above does not teach the gray voltage generator separately storing gray voltages for each voltage polarity.

However, Kudo [fig. 13] further teaches a gray voltage generator generating gray voltage signals that are specific to different voltage polarities.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the signal controller of Park as modified above to include a register storing gamma values for each of different voltage polarities and to modify the gray voltage generator of Park as modified above to generate gray voltage signals that are specific to different voltage polarities by including additional memory, decoder, and D/A converter for each of the different voltage polarities such that the gray voltage generator of Park as modified above separately stores gray voltages for each voltage polarity, as taught by Kudo, in order to supply gray voltages representing more accurate gamma curves to the liquid crystal panel of the display of Park as modified above, and thus to improve the image quality of the display.

As to **claim 9**, Park as modified by Kudo teaches the gray voltage generator (Park: a combination of "*memory 32*", "*decoder 33*", and "*D/A converter 34*" included in a plurality of "*column driver IC 14*") [Park: figs. 1 and 3] being coupled to the data driver (Park: a combination of "*shift register 24*", "*data latch 26*", "*d/a converter 28*", and "*buffer 30*" included in a plurality of "*column driver IC 14*") [Park: figs. 1 and 3] by a plurality of buses.

As to **claim 10**, Park as modified by Kudo teaches that the signal controller (Park: "*controller 20*") comprises a register (Kudo: "*controller register 301*") [Kudo: fig. 16] for storing a predetermined number of digital gamma data, wherein the digital gamma data are supplied to the gray voltage generator for generating independent gamma curves for the different pixel colors [Kudo: par. (0107) lines 1-4 and par. (0108) lines 6-10].

As to **claim 11**, Park as modified by Kudo teaches a gate driver (Park: a combination of "*scan driver IC 12*") [Park: fig. 1] coupled to the signal controller (Park: "*controller 20*"), wherein the gate driver generates gate control signals in response to signals from the signal controller [Park: par. (0028) lines 7-9 and par. (0030) lines 8-9].

As to **claim 12**, Park teaches a liquid crystal panel assembly [par. (0026) lines 1-3] comprising:

a plurality of pixel electrodes (a combination of "*scan lines*" and "*column lines*"), wherein each of the pixel electrodes is associated with a pixel color (image data having different pixel colors are supplied to column lines as shown in fig. 3);

a data driver (a combination of "*shift register 24*", "*data latch 26*", "*d/a converter 28*", and "*buffer 30*" included in a plurality of "*column driver IC 14*") [figs. 1 and 3] for supplying data signals to the pixel electrodes ("*column lines*"); and

a gray voltage generator (a combination of "*memory 32*", "*decoder 33*", and "*D/A converter 34*" included in a plurality of "*column driver IC 14*") [figs. 1 and 3] coupled to the data driver, wherein the gray voltage generator generates gray voltages so that the data driver determines a particular data signal for a particular pixel electrode by using one of the gray voltages [par. (0037)].

Park does not expressly disclose a common electrode and a liquid crystal layer.

However, Examiner takes official notice that it is well known in the art to include a common electrode positioned substantially parallel to pixel electrodes and a liquid crystal layer positioned between the pixel electrodes and the common electrode, in a liquid crystal display.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a common electrode and a liquid crystal layer in such ways, in order to rotate the liquid crystals of the display by applying voltages between pixel electrodes and a common electrode.

Park does not teach the gray voltage generator generating gray voltages that are each associated with a pixel color and the data driver determines a data signal by using one of the gray voltages that is associated with the pixel color of the particular pixel electrode.

However, Kudo teaches an apparatus for driving a liquid crystal display [par. (0002)] comprising a signal controller (a combination of "*MPU 906*", "*system interface 907*", and "*control register 301*") [fig. 16] generating digital signals, gray scale voltage generator ("*302*") coupled to the signal controller generating gray voltage signals that are each associated with a pixel color [par. (0107) lines 1-4 and par. (0108) lines 6-10], and a data driver ("*decoder circuit 303*") determining a data signal by using one of the gray voltages that is associated with the pixel color.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the signal controller of Park to include a register storing gamma values for each of a plurality of pixel colors, to modify the gray voltage generator of Park to generate gray voltage signals that are each associated with a pixel color by including additional memory, decoder, and D/A converter for each of the plurality of pixel colors, and to modify the data driver of Park to select one of the gray voltage signals which is associated with the same pixel color, as taught

by Kudo, in order to supply gray voltages representing more accurate gamma curves to the liquid crystal panel of the display of Park, and thus to improve the image quality of the display.

As to **claim 13**, all of the claim limitations have already been discussed with respect to the rejection of claim 2.

As to **claim 21**, all of the claim limitations have already been discussed with respect to the rejection of claim 9.

As to **claim 22**, all of the claim limitations have already been discussed with respect to the rejection of claim 1.

As to **claim 23**, all of the claim limitations have already been discussed with respect to the rejection of claim 2.

7. **Claims 3, 4, 6, 8, 14, 15, 17, 19, 20**, and **24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Kudo as applied to claims 1, 2, 9, 10-13, and 21-23 above, and further in view of Uehara et al. (US 5,663,772, herein after "Uehara").

As to **claim 3**, Park as modified by Kudo [Park: fig. 3] teaches a gray voltage generator (Park: a combination of "*memory 32*", "*decoder 33*", and "*D/A converter 34*" included in a plurality of "*column driver IC 14*") [Park: figs. 1 and 3].

Park as modified by Kudo does not teach the gray voltage generator to include a first color-specific gamma voltage register and a second color-specific gamma voltage register.

However, Uehara [fig. 1] teaches an idea of including a first register ("*1031*") and a second register ("*1032*") in a driving circuitry of a display in order to temporarily store image related data before the data is processed [col. 6 lines 53-58].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the gray voltage generator of Park as modified by Kudo to include a first register and a second register between the decoder of Park as modified by Kudo and the D/A converter of

Park as modified by Kudo so that the data transferred from the decoder are temporality stored in the registers before the data is processed to D/A converter, as taught by Uehara, in order to allow the gray voltage generator of Park as modified by Kudo to supply gamma voltages to the data driver of Park as modified by Kudo at proper timings, and thus to allow the data driver to convert digital image data to analog signals properly.

As to **claim 4**, Park as modified by Kudo and Uehara teaches the gray voltage generator further comprising a digital-to-analog converter (Park: "*34*") [Park: fig. 3] for converting the digital gamma voltages that are stored in the first and the second color-specific gamma voltage registers into analog gray voltages.

As to **claim 6**, Park as modified by Kudo and Uehara teaches that the data driver (Park: a combination of "*shift register 24*", "*data latch 26*", "*d/a converter 28*", and "*buffer 30*" included in a plurality of "*column driver IC 14*") [Park: figs. 1 and 3] comprises a plurality of data driving circuits for receiving image data ("*R,G,B data*") and data control signals ("*column control signal*") from the signal controller (Park: "*controller 20*") [Park: fig. 1] [Park: par. (0037)], wherein each of the data driving circuits (Park: a combination of "*shift register 24*", "*data latch 26*", "*d/a converter 28*", and "*buffer 30*") [Park: fig. 3] includes a sampling unit (Park: a combination of "*D/A converter 28*" and "*buffer 30*") for sampling gamma voltage data from the digital-to-analog converter (Park: "*D/A converter 34*").

As to **claim 8**, Park as modified by Kudo and Uehara teaches the image data being transmitted from the signal controller (Park: "*controller 20*") [Park: fig. 1] to the data driving circuits (Park: a combination of "*shift register 24*", "*data latch 26*", "*d/a converter 28*", and "*buffer 30*" included in each of a plurality of "*column driver IC 14*") [Park: figs. 1 and 3] by two signal lines that are separately connected between the data driving circuits and the signal controller.

As to **claim 14**, all of the claim limitations have already been discussed with respect to the rejection of claim 3.

As to **claim 15**, all of the claim limitations have already been discussed with respect to the rejection of claim 4.

As to **claim 17**, all of the claim limitations have already been discussed with respect to the rejection of claims 1 and 6.

As to **claim 19**, all of the claim limitations have already been discussed with respect to the rejection of claim 8.

As to **claim 20**, all of the claim limitations have already been discussed with respect to the rejection of claim 10.

As to **claim 24**, all of the claim limitations have already been discussed with respect to the rejection of claims 1 and 10.

6. **Claims 5** and **16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Park, Kudo, Uehara as applied to claims 3, 4, 6, 8, 14, 15, 17, 19, 20, and 24 above, and further in view of Van Mourik (US 6,215,468, herein after "Van").

As to **claim 5**, Park as modified by Kudo and Uehara teaches that the first color-specific gamma voltage register and the second color-specific gamma voltage register are connected by buses, and at least one of the first and second color-specific gamma voltage registers is connected to the digital-to-analog converter by buses [Park: fig. 3] (Park: "*m-bit*").

Park as modified by Kudo and Uehara does not teach the buses being ten-bit buses.

However, Van teaches an apparatus for driving a liquid crystal display [col. 4 lines 58-61] processing 10-bit gamma data [fig. 1].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the apparatus of Park as modified by Kudo and Uehara to use 10-bit buses such that

10-bit gamma data is used for gamma correction, as taught by Van, in order to correct the discrepancy between each of the pixel colors more accurately.

As to **claim 16**, all of the claim limitations have already been discussed with respect to the rejection of claim 5.

7. **Claims 7** and **18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Park, Kudo, Uehara as applied to claims 3, 4, 6, 8, 14, 15, 17, 19, 20, and 24 above, and further in view of Kitajima et al. (US 5,091,722, herein after "Kitajima").

As to **claim 7**, Park as modified by Kudo and Uehara teaches the sampling unit (Park: a combination of "*D/A converter 28*" and "*buffer 30*" included in a plurality of "*column driver IC 14*") [Park: fig. 1] comprising a plurality of sampling circuits.

Park as modified by Kudo and Uehara does not expressly disclose the structure of the sampling circuit.

However, Kitajima [fig. 13] teaches a sampling circuit ("*3*") included in a display apparatus, which comprises:

a switch ("*8*", "*9*", and "*10*") that turns on in response to a sampling signal from a signal controller;

a capacitor coupled to the switch for storing the sampled gamma voltage data ("*17*", "*18*", and "*19*"); and

an analog buffer ("*20*", "*21*", and "*22*") coupled to the capacitor for outputting the stored gamma voltage data.

It would have been obvious to one of ordinary skill in the art at the time of the invention to specify the structure of the sampling circuit of Park as modified by Kudo and Uehara to include a switch, a capacitor, and an analog buffer, as taught by Kitajima, in order to reduce the

number of components required to build a sampling circuit, and thus to simplify the driving circuitry of the sampling circuit.

As to **claim 18**, all of the claim limitations have already been discussed with respect to the rejection of claim 7.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (572) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

04/25/2007

- s.m.

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